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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,033	07/03/2003	Tadashi Iguchi	03180.0326	5852

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,033	IGUCHI ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-13,16 and 17* is/are rejected.

7)☒ Claim(s) *4,5,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 July 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 6 states that the wordline and the control electrode are on the "same conductive layer." However the examiner believes that the control gate and the wordline are the exact same structure in the applicant's invention. The specification does not appear to suggest a separate control gate and a separate wordline. Therefore the metes and bounds of claim 6 are unclear to the examiner.

5. Claim 7 states that the insulating film (which is in the second trench) and the gate insulating film are on the "same insulating layer." However the examiner believes that the insulating film (which is in the second trench) and the gate insulating film are the exact same layer in the applicant's invention. The specification does not appear to

suggest a separate insulating film (which is in the second trench) and a separate gate insulating film. Therefore the metes and bounds of claim 7 are unclear to the examiner.

6. Claim 8 recites the limitation "said gate insulating film" in the first line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-3, 6-11, 12, 13, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Aritome (USPN 5,949,101).

9. In reference to claim 1, Aritome (USPN 5,949,101) discloses a similar device. Figure 6A discloses a non-volatile semiconductor memory device arranged in a matrix on a semiconductor substrate (1A). Each cell in the matrix has a floating gate or electrode (4). There are element isolating regions (2); each of which has a first trench, filled with an isolating filler, that is formed in the semiconductor substrate and between the memory cells adjacent each other along a gate width direction. There is a second trench formed in the isolating filler between the floating gates (4) of the memory cells adjacent to each other along the gate width direction. The second trench is narrow at the bottom. A word line (6), buried in the second trenches, is connected to the memory cells and extends along the gate width direction.

10. In reference to claim 2, Aritome meets the limitation of the claim. The applicant has disclosed that the parasitic capacitance can be reduced if the second trench is shallower than the first trench and preferably reaches the surface of the well region (p. 9, lines 17-21 of applicant's specification). The Aritome device illustrated in figure 6A meets these specified features.

11. In reference to claim 3, the second trench is in the shape of a V.

12. So far as understood in claim 6, there is a control electrode or control gate (6) with a gate insulating film (33) provided on the floating gate (4). The control gate (6) acts as the wordline and both are therefore of the same material and in the same conductive layer.

13. So far as understood in claim 7, the control gate or wordline (6) is buried in the second trench via an insulating film (33). This insulating film (33) acts as the gate insulating film (33); therefore the insulating film and the gate insulating film are on the same insulating layer.

14. So far as understood in claim 8, Aritome discloses that the gate insulating film (32) may be made of silicon nitride (claims 11 and 16 in column 16).

15. In reference to claim 9, the first and second trenches of Aritome have approximately the same top diameter. However the second trench of Aritome has bottom diameter which is smaller than that of the first trench. Thus Aritome has ratio of a top diameter to a bottom diameter of the second trench is large compared to the ratio of a top diameter to a bottom diameter of the first trench.

16. In reference to claim 10, the second trench is shallower than the first trench and extends below a surface of the semiconductor substrate (1A).

17. With regard to claim 11, the non-volatile memory device in figure 6A is of the NAND type electrically erasable programmable read only memory (column 7, lines 20-25).

18. In reference to claims 12, 13, and 16, the fabrication process of the Aritome device illustrated in figure 6A inherently meets these claims.

19. Claims 1-3, 6, 8-11, 12, 13, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Aritome (USPN 5,949,101).

20. In reference to claim 1, Aritome (USPN 5,949,101) discloses a similar device. Figure 12G discloses a non-volatile semiconductor memory device arranged in a matrix on a semiconductor substrate (40). Each cell in the matrix has a floating gate or electrode (30). There are element isolating regions (12); each of which has a first trench, filled with an isolating filler, that is formed in the semiconductor substrate and between the memory cells adjacent each other along a gate width direction. There is a second trench formed in the isolating filler between the floating gates (30) of the memory cells adjacent to each other along the gate width direction. The second trench is narrow at the bottom. A word line (75), buried in the second trenches, is connected to the memory cells and extends along the gate width direction.

21. In reference to claim 2, Aritome meets the limitation of the claim. The applicant has disclosed that the parasitic capacitance can be reduced if the second trench is shallower than the first trench and preferably reaches the surface of the well region (p.

9, lines 17-21 of applicant's specification). The Aritome device illustrated in figure 12G meets these specified features.

22. In reference to claim 3, the second trench is in the shape of a V.

23. So far as understood in claim 6, there is a control electrode or control gate (72, 75) with a gate insulating film (71) provided on the floating gate (30). The control gate (72, 75) acts as the wordline and both are therefore of the same material and in the same conductive layer.

24. So far as understood in claim 8, Aritome discloses that the gate insulating film (71) may be made of an ONO layer, which contains silicon nitride (column 10, lines 20-26).

25. In reference to claim 9, the first and second trenches of Aritome have approximately the same top diameter. However the second trench of Aritome has bottom diameter which is smaller than that of the first trench. Thus Aritome has ratio of a top diameter to a bottom diameter of the second trench is large compared to the ratio of a top diameter to a bottom diameter of the first trench.

26. In reference to claim 10, the second trench is shallower than the first trench and extends below a surface of the semiconductor substrate (40).

27. With regard to claim 11, the non-volatile memory device in figure 12G is understood to be a NAND type electrically erasable programmable read only memory.

28. In reference to claims 12, 13, and 16, the fabrication process of the Aritome device illustrated in figures 12A-12G inherently meets these claims.

29. In reference to claim 17, the fabrication process of the Aritome device illustrated in figures 12A-12G inherently meets this claim. Claim 17 is similar to claim 12 with the exception that a spacer is disclosed as being used as a mask for the formation of the second trench. Figure 12E of Aritome illustrates the use of a spacer which acts as a mask for the formation of the second trench. Therefore the fabrication process shown in figures 12A-12G meets this claim.

Allowable Subject Matter

30. Claims 4, 5, 14, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

31. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a semiconductor non-volatile memory device with a floating gate embedded within a trench formed within the trench insulation structures which isolate each memory cell where the trench has the shape of a U or an inverted trapezoid.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ